University of Colorado Boulder
ECEE Department

ECEN 2350 - Digital Logic - Fall 2023
Location: Engineering Center, ECCR 1B40, MWF 1:25PM - 2:15PM
Instructor: Dr. Mona ElHelbawy
Lab #10: Simulate Glitch and Delay
Date of Experiment: November 30th, 2023
Names: Connor Sorrell

Description

In this lab, we will examine the delay in combinational circuits, specify the delay of each gate in SystemVerilog and simulate the circuits to see how delay can affect the behavior of a combinational circuit.

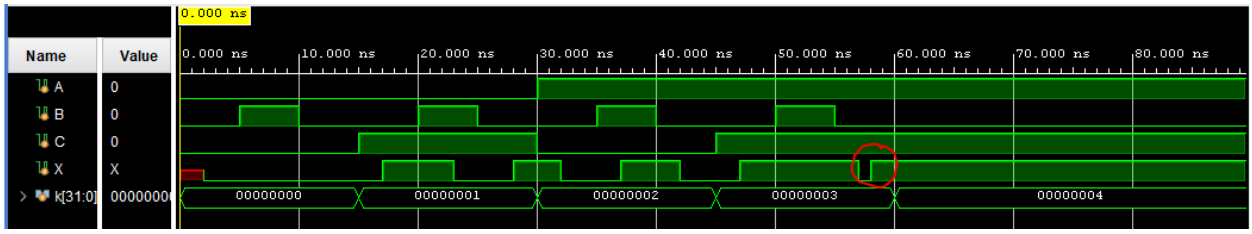

Figure 1.0.1: Shows the simulation results of the circuit where all gates have a delay of 1ns.

Now that I have completed part 1 of the lab, I will try the following modifications.

First off, I will change the propagation delay of the OR gate from 1ns to 2ns. To do this, I will change the design file code.

Edited Design File Code

```
`timescale 1ns / 1ps
module CombCirc(
input A,
input B,
input C,
output logic X
);
logic N1, N2, N3;
// AND gate with 1ns delay
always_comb N1 <= #1 A & B;
// Not Gate with 1ns delay
always_comb N2 <= #1 ~B;
// And Gate with 1ns delay
always_comb N3 <= #1 N2 & C;
// Or Gate with 2ns delay
always_comb X <= #2 N1 | N3;
endmodule
```

Upon simulating the circuit again, there is a glitch present after 58ns which lasts 1ns. The biggest change I notice from this simulation is that now the toggle from B going from 1 to 0 just takes slightly longer to propagate.

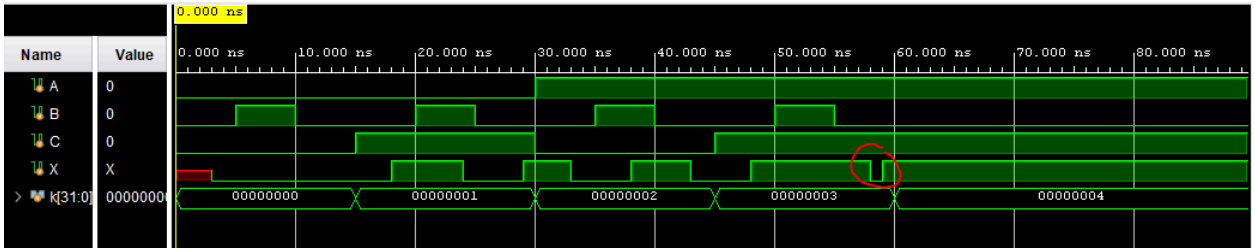

Figure 1.0.2: Shows the simulation of the circuit after changing the OR gate to a 2ns delay, with a red circle highlighting the glitch at 58ns.

Now, I will change the delay of all gates to 5ns.

Edited Design Code for 5ns delay of all gates

```
`timescale 1ns / 1ps
module CombCirc(
input A,
input B,
input C,
output logic X
);
logic N1, N2, N3;
// AND gate with 1ns delay
always_comb N1 <= #5 A & B;
// Not Gate with 1ns delay
always_comb N2 <= #5 ~B;
// And Gate with 1ns delay
always_comb N3 <= #5 N2 & C;
// Or Gate with 2ns delay
always_comb X <= #5 N1 | N3;
Endmodule
```

After simulating the circuit with a 5ns delay for all gates, there still exists a glitch. The glitch starts at 65 ns and has a duration of 5ns. This is because instead of glitch processing right after the B toggles, the not gate now has a 5ns delay so the circuit takes 5x as long to process.

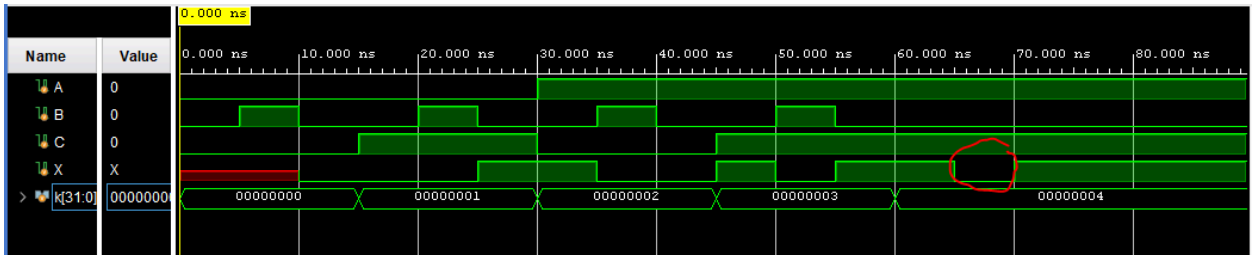

Figure 1.0.3: Shows the simulation of the circuit after changing each gate to a 5ns delay, with a red circle highlighting the glitch.